

Description

APPARATUS AND METHOD FOR GENERATING A PHASE DELAY

BACKGROUND OF INVENTION

[0001] 1. Field of the Invention

[0002] The present invention relates to an apparatus for generating a phase delay, and more specifically, to an apparatus for generating a phase delay, which can compensate a phase difference between input signals.

[0003] 2. Description of the Prior Art

[0004] Many types of circuits, such as clock generators or RF transceivers, require signals with phase of high precision because imprecise signal phases have a large impact on the whole system performance. In regards to a multi-phase clock generator, the precision of each output signal phase is also very important. The larger the phase error is, the larger the jitter of output clock signal(s) may be. For systems in need of precise clock signals, such jitter may

result in serious performance degradation in circuits of the following stages, such as erroneous sampling operation of an ADC (analog to digital converter) or an increased bit error rate.

[0005] When designing a circuit, it is necessary to be very cautious when considering routing paths that involve signals in need of highly precise signal phases. However, because a number of factors, such as temperature, manufacturing process variations and fluctuations in supply voltage, cannot be completely controlled, conventional VLSI circuits alone usually cannot provide precise phase delays, necessitating the use of additional mechanisms to correct the shifts in signal phases.

[0006] One of the techniques of phase adjusting is, by charging/discharging a capacitor, to insert an RC delay to a signal transmitted to circuits in the next stage. In general, a plurality of switches are respectively utilized to connect/disconnect a plurality of capacitors, so as to adjust the capacitance value, and the capacitance value in conjunction with a buffer is utilized to provide an RC delay to delay the phase of the signal.

[0007] Please refer to Fig.1. OLE_LINK1Fig.1 shows a block diagram of such a typical apparatus 100 for generating a

phase delay. OLE_LINK1 The apparatus 100 contains a plurality of capacitors, a plurality of switches, and a buffer, and is utilized to generate an output signal by delaying an input signal. By turning on different combinations of switches, the capacitance value seen at a node N of the circuit can be adjusted. Turning on more switches results in a higher capacitance value at the node N, which in turn increases the amount of phase delay in the input signal.

[0008] In order to precisely control the phase delay of the transmitted signal, it is desirable that the capacitance and the resistance of the above-mentioned plurality of switches are of such insignificant values that they can be ignored when compared to the capacitance value of the plurality of capacitors and the resistance value of the buffer. Reason being if the parasitic capacitance value and resistance value brought by the switches are too large, the amount of RC delay may deviate from designated values, which is not desirable in circuit operation.

[0009] However, along with advances in technologies, a need for even further fine control of signal phase delay emerges, which in turn necessitate the use of devices (capacitors, buffers, etc) with even smaller resistance and capacitance in facilitating the RC delay. Under such circumstances,

switches implemented by MOS transistors face the following dilemma: in order to minimize the capacitance value of the switch, the size of the MOS transistor needs to be as small as possible; on the other hand, in order to minimize the resistance value of the switch, the size of the same MOS transistor needs to be as large as possible. Hence, such dilemma results in difficulties in the design of the apparatus 100.

SUMMARY OF INVENTION

[0010] It is therefore one of the many objectives of the claimed invention to provide an apparatus and a method for converting a digital value representative of a phase delay to a control voltage, in order to control a variable capacitor and a buffer, so as to generate an output signal by delaying an input signal.

[0011] According to an embodiment of the claimed invention, an apparatus for generating a phase delay is disclosed. The apparatus comprises a buffer for buffering an input signal and outputting an output signal; a DAC for outputting a control voltage corresponding to a digital value representative of a phase delay; and a variable capacitor coupled to the DAC and the buffer, the capacitance value of the variable capacitor corresponding to the control voltage;

wherein by controlling the capacitance value, the apparatus adjusts the phase delay between the input signal and the output signal.

[0012] According to another embodiment of the present invention, a method for generating a phase delay is also disclosed. The method comprises the following steps:
buffering an input signal to generate an output signal;
providing a digital value representative of a phase delay;
generating a control voltage corresponding to the digital value representative of the phase delay; adjusting a capacitance value of a variable capacitor with the control voltage, to adjust the phase delay between the input signal and the output signal.

[0013] These and other objectives of the claimed invention will no doubt become obvious to those of ordinary skill in the art after reading the following detailed description of the embodiment, which is illustrated in the various figures and drawings.

BRIEF DESCRIPTION OF DRAWINGS

[0014] Fig.1 shows the block diagram of a typical apparatus for generating a phase delay.

[0015] Fig.2 is a functional block diagram of an apparatus for generating a phase delay according to an embodiment of

the claimed invention.

[0016] Fig.3 is a flowchart of a delaying process employed by the apparatus for generating a phase delay according to an embodiment of the claimed invention.

DETAILED DESCRIPTION

[0017] Please refer to Fig.2. Fig.2 is a functional block diagram of the apparatus 200 for generating a phase delay to delay a signal according to an embodiment of the claimed invention. The apparatus 200 for generating a phase delay in Fig.2 contains a buffer 20, a DAC 21, and a variable capacitor 22. The buffer 20 has an input end and an output end and is utilized for buffering an input signal received by the input end and generating an output signal outputted by the output end. The input signal received by the buffer 20 is usually a clock signal outputted by a clock generator or a signal outputted by an RF transceiver. The DAC 21 has an input end and an output end and is utilized to convert a digital value representative of a phase delay received by the input end into a control voltage outputted by the output end. The variable capacitor 22 has two ends. One end is electrically coupled to the output end of the DAC 21, and the other end is electrically coupled to the output end of the buffer 20, where the capaci-

tance value of the variable capacitor 22 is determined according to the control voltage. As an embodiment, the variable capacitor 22 can be a MOS-based voltage-controlled capacitor (or a varactor), or a P+/N well junction voltage-controlled capacitor, which are well-known to those of ordinary skill in the art.

[0018] It is to be noted that two or more of the above-mentioned circuits of the claimed invention can also be implemented at the same time. In the case of two, the two circuits can respectively adjust the phases of two input signals (one input signal per circuit) in order to adjust the phase difference between the input signals, wherein the two input signals may be a pair of differential signals, or I/Q signals of a receiver and/or a transmitter of communication systems.

[0019] Fig.3 is a flowchart of a delaying process employed by the apparatus 200 for generating a phase delay according to an embodiment of the claimed invention. The flow process includes the following steps:

[0020] Step 200: Start;

[0021] Step 202: The input end of the buffer 20 receives an input signal;

[0022] Step 204: The input end of the DAC 21 receives a digital

value representative of a phase delay. The DAC 21 converts the digital value into a corresponding control voltage and then outputs the control voltage with the output end;

[0023] Step 206: The variable capacitor 22 receives the control voltage, and the control voltage controls the variable capacitor 22 and adjusts the variable capacitor 22 to have a capacitance value corresponding to the digital value representative of the phase delay;

[0024] Step 208: Use the variable capacitor 22 and the buffer 20 to provide an RC delay, so as to delay the input signal. Then, the output signal is outputted by the output end of the buffer 20; and

[0025] Step 210: End the operation of generating the phase delay, and finish the process according to the embodiment.

[0026] The capacitance value of the variable capacitor 22 varies with the control voltages (the control voltages is the value of voltage across the variable capacitor). Hence, if the voltage across the variable capacitor is controlled with a certain precision, the capacitance value with corresponding resolution can be acquired. With the state of the art technology, it is not difficult to generate a control voltage with a much higher resolution by controlling the variable capacitor with a DAC. Therefore, the precision of the

phase delay can be significantly increased. In addition, since the value representative of the phase delay received by a DAC is recorded digitally, there can be a number of various detecting methods that can be used for detecting the phase difference in the previous stage.

[0027] Those skilled in the art will readily observe that numerous modifications and alterations of the device may be made while retaining the teachings of the invention. Accordingly, the above disclosure should be construed as limited only by the metes and bounds of the appended claims.